

SN. 10/797,923

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**REMARKS**

Applicant respectfully requests that the foregoing amendments be made prior to examination of the present application, and respectfully requests reconsideration of the present application in view of the foregoing amendments and the reasons that follow.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Claims 1-13 are pending. Claims 1-13 are subject to restriction. Claims 1-9 were elected for initial prosecution. Claims 10-13 are claims for a method of manufacturing a device as in claims 1-9. Therefore, they are properly examined in the present application once allowable subject matter has been agreed upon with respect to the product claims 1-9, under the doctrine set forth in *In re Ochiai*.

Claims 1, 4 and 10 have been amended to recite "a first conduction type high concentration impurity layer directly underlying said low concentration impurity layer." Support for this is found in the drawings.

Claims 6 and 9 are indicated as allowable and have been rewritten in independent form. Accordingly, claims 6 and 9 are in *prima facie* condition for allowance.

Claims 1-5, 7 and 8 are rejected under Section 102(b) based on Bosselaar *et al.* (U.S. 4,148,053). The examiner urges that

With regard to claims 1-3, Bosselaar *et al.* discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 1 formed beneath a principal face of a wafer to a predetermined depth; a first conduction type high concentration impurity layer 2 having an impurity concentration (note column 4 lines 19-20) of  $5 \times 10^{19}/\text{cc}$  (and thus, inherently, resistance value not higher than  $0.05 \Omega \cdot \text{cm}$ , note figure 6 of Kroger 4,544,937) underlying said low concentration impurity layer 1; and a first conduction type high concentration impurity diffusion region 6 having a lattice-shaped pattern (Note figure 2 of Rowe 4,040,878, which is incorporated by reference into Bosselaar *et al.* at column 4 line 60), formed along at least a portion of the

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dicing lines A-A that delimit a plurality of chips (again, the plurality of chips is seen most clearly in figure 2 of Rowe 4,040,878, which is incorporated by reference into Bosselaar *et al.*) on said wafer, said diffusion region 6 extending from the principal face of the wafer to said high concentration impurity layer 2, wherein said diffusion region 6 has a width larger than that of the cutting allowance for the dicing along the dicing lines A-A. Note figures 4-6, column 4 lines 19, 20, and 49-64, column 5 lines 56-60, and column 6 lines 35-39 of Bosselaar *et al.*

Claims 1, 4 and 10 have been amended to recite that the first conduction type high concentration impurity layer directly underlies the low concentration impurity layer. In Bosselaar *et al.*, layer 3 is positioned between layers 1 and 2. Accordingly, claims 1-5, 7 and 8 differ significantly from Bosselaar *et al.* and would not have been obvious based on the cited document.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

If there are any problems with this response, Applicant's attorney would appreciate a telephone call. In view of the foregoing, it is believed none of the references, taken singly or in combination, disclose the claimed invention. Accordingly, this application is believed to be in condition for allowance, the notice of which is respectfully requested.

Respectfully submitted,

ROSSI, KIMMS & McDOWELL LLP



MARC A. ROSSI  
REG. NO. 31,923

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DATE

P.O. Box 826  
ASHBURN, VA 20146-0826  
703-726-6020 (PHONE)  
703-726-6024 (FAX)